N channel 100V MOSFET

1. Description

The HS15N10DA is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance.These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits,and low in-line power loss that are needed in a very small outlinesurface mount package.

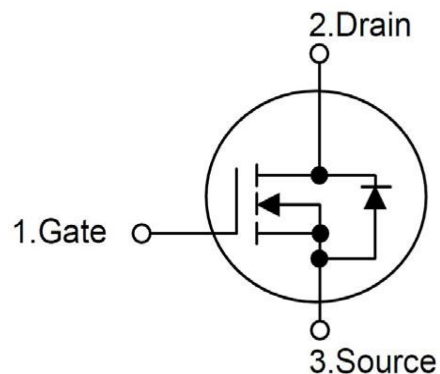
2. Feature

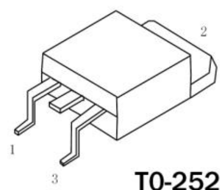
- $R_{DS(ON)} \leqq 100m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current

V_{DS}	100	V
$R_{DS(on)}$	100	mΩ
I_D	15	A

3. Pin configuration

Order Number	Package
HS15N10DA	T0-252





T0-252

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4. Absolute maximum ratings (Tc=25℃ Unless Otherwise Noted)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	15	A
	Tc=70℃		14	A
Pulsed Drain Currenta		I_{DM}	59	A
Power Dissipation	Tc=25℃	P_D	34.7	W
	Tc=70℃		22.2	
Operating Junction and Storage Temperature Range		T_J, Tstg	-55~+150	℃

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	R_{thCS}	0.5	°C/W
Thermal resistance junction to case.	R_{thJC}	3.6	°C/W
Thermal resistance junction to ambient.	R_{thJA}	110	°C/W

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6. Electrical characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	–	–	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=VGS, I_D=250μA	1	–	3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V	–	–	±100	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V	–	–	1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=8A	–	80	100	mΩ
V_{SD}	Diode Forward Voltage	I_S=8A, V_{GS}=0V	–	0.9	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DD}=80V, V_{GS}=10V, I_D=10A	–	13	–	nC
Q_{gs}	Gate-Source Charge		–	4.6	–	
Q_{gd}	Gate-Drain Charge		–	7.6	–	
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	–	890	–	pF
C_{oss}	Output Capacitance		–	58	–	
C_{rss}	Reverse Transfer Capacitance		–	23	–	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=50V, R_G=1Ω, R_L=5 Ω,V_{GEN}=10V	–	14	–	ns
t_r	Turn-On Rise Time		–	33	–	
$t_{d(off)}$	Turn-Off Delay Time		–	39	–	
t_f	Turn-Off Fall Time		–	5	–	
I_{SD}	Continuous drain-source current		–	–	15	A
I_{SM}	Pulsed drain-source current		–	–	59	A

Notes :a. pulse test:pulse width 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

b. HOMSEMI reserves the right to improve product design,functions and reliability without notice.

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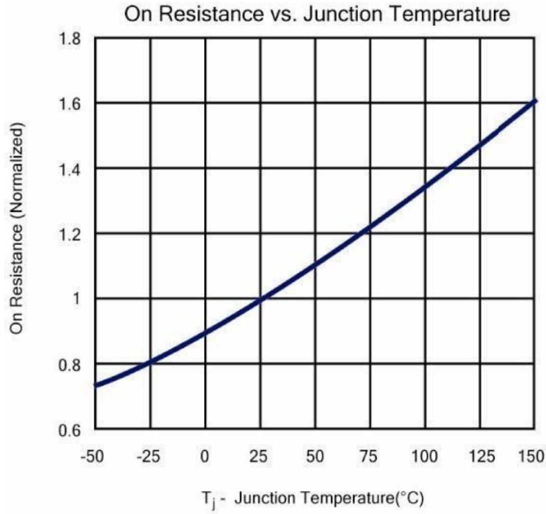
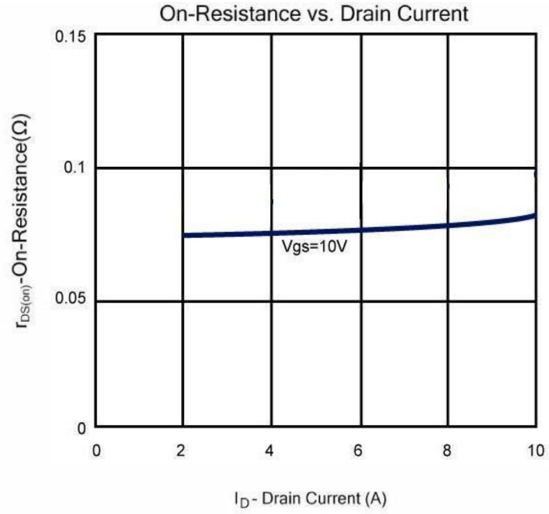
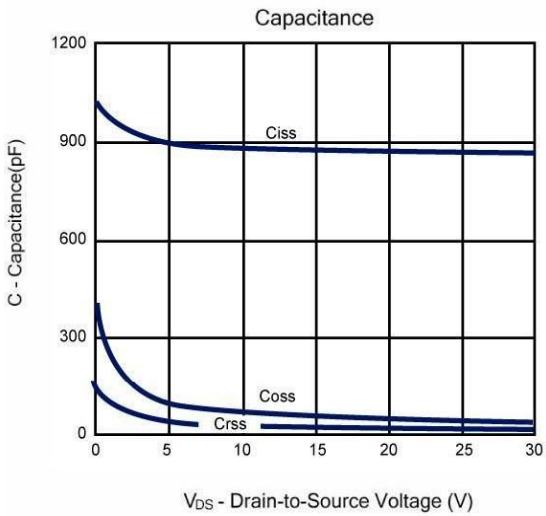
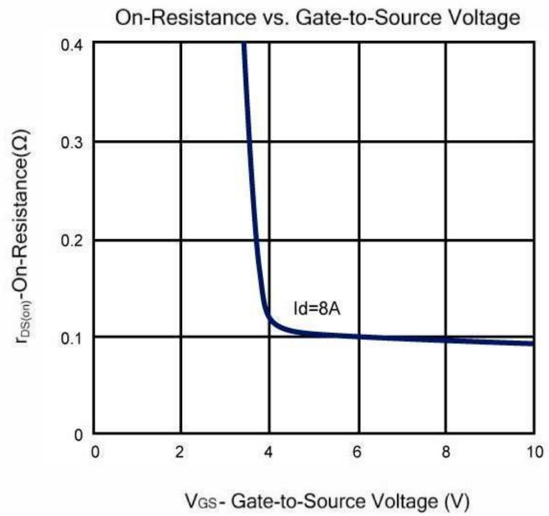
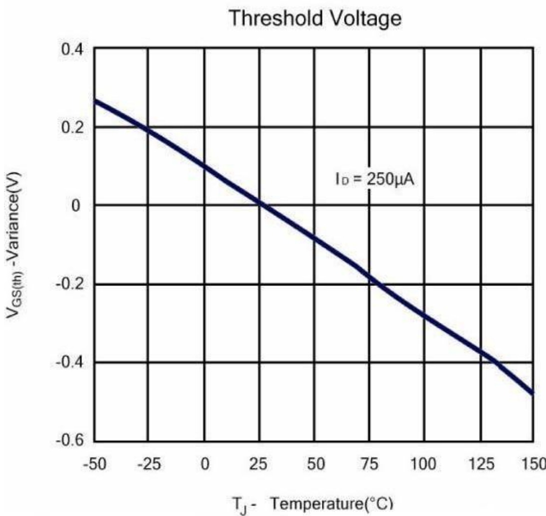
7. Typical Characteristics (TJ =25℃ Noted)

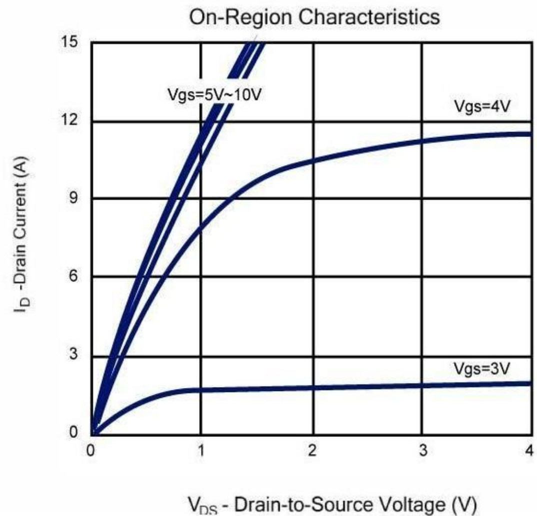












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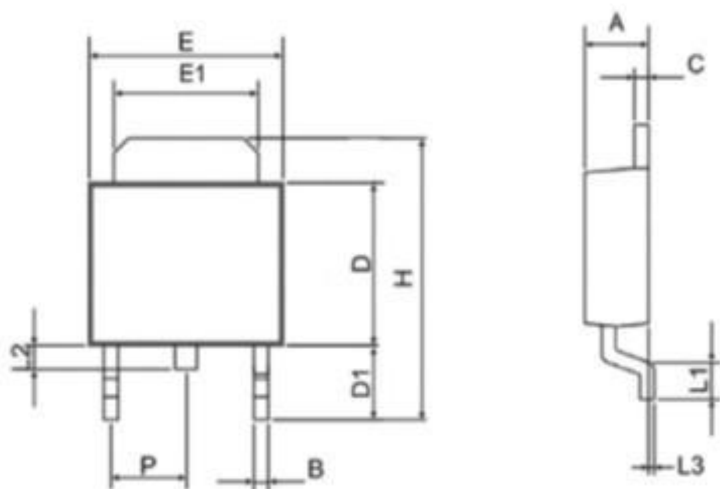
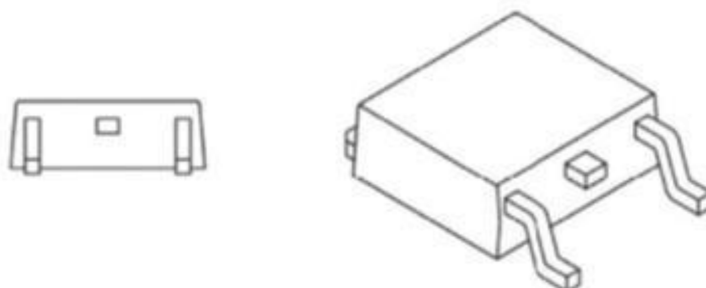
8.Package Information：

Unit：mm



SYMBOL	MIN	MAX
A	2.1	2.5
B	0.4	0.9
C	0.4	0.9
D	5.3	6.3
D1	2.2	2.9
E	6.3	6.75
E1	4.8	5.5
L1	0.9	1.8
L2	0.5	1.1
L3	0	0.2
H	8.9	10.4
P	2.30 BSC	



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